PI3HDMI1210-A
PI3HDMI1210-A Sink Application with HDCP Support

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1 Introduction

PI3HDMI1210-A is a high-performance 2:1 Mux switch which maximum data rate of 4.0Gbps provides resolution for next generation PC graphics and HDTV. It is a one-chip solution that offers four differential channels and two side-band channels. Customers can have the opportunity to connect Serial Data and Clock signals in parallel with four differential signal pairs to PI3HDMI1210-A. Reference schematic using PI3HDMI1210-A for sink application are studied in this application note.

2 Typical Application Circuit

Two reference design circuits are presented below. In Application 1, sink application with HPD reset is studied. In Application 2, sink application with HPD reset and RxSense feature is introduced.

2.1 Application 1: Sink Application with HPD Reset

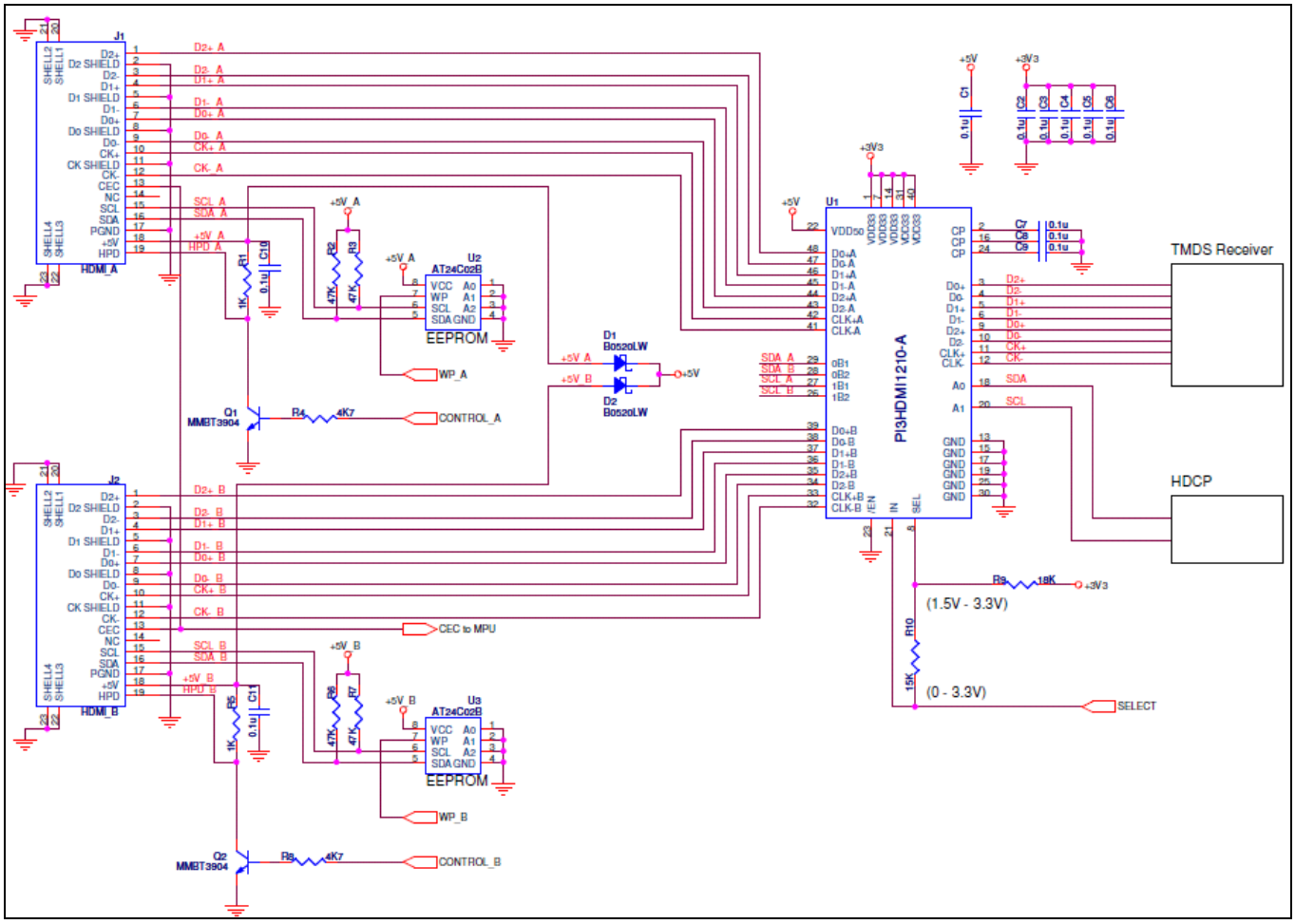

Figure 1: PI3HDMI1210-A Sink Reference Schematic with HPD Reset

With two HDMI ports connected to PI3HDMI1210-A, one of them can be selected using two control pins, SEL and IN pins. HPD reset circuitry is implemented in the reference schematic shown above. The function of HPD reset will be discussed shortly.

The control pin, namely SEL of PI3HDMI1210-A, is used to control port selection for high speed differential signals. The operating range of SEL is from 1.5V to 3.3V. The IN control pin is used to select port for sideband DDC signals. It operates between 0 and 3.3V. The waveforms of SEL and IN are shown below.

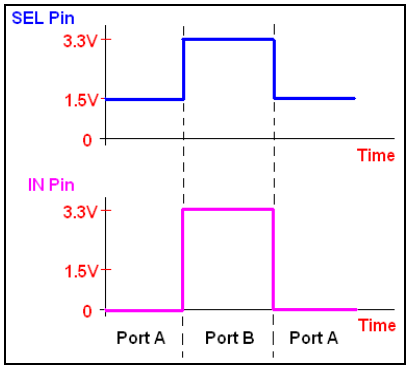

Figure 2: PI3HDMI1210-A Port Selection Voltage

Each TMDS sink device contains CEA-861-D compliant EEPROM. A TMDS source device reads the EDID content of the sink device stored in the EEPROM in order to discover the configuration of the sink device.

High-bandwidth Digital Content Protection (HDCP) key can be retrieved from the EDID. HDCP is used for controlling digital audio and video contents as signals travel across TMDS connections. The source device and the sink device will exchange the "HDCP' keys before delivering digital audio and visual data. Each HDCP capable source device or sink device has a unique set of keys, i.e. 40 keys of 56-bit long.

Because of unique set of keys, when selection of transmitters attached to PI3HDMI1210-A is switched from one port to another, the receiver has to be initiated to read the HDCP of transmitter again. Figure 2.5 of High-bandwidth Digital Content Protection System Specification Rev.1.4 (which is shown in the figure below) states that resetting HPD can cause the sink device to go through states H0 to H2 and read EDID to check whether the source is a DVI transmitter or an HDMI transmitter.

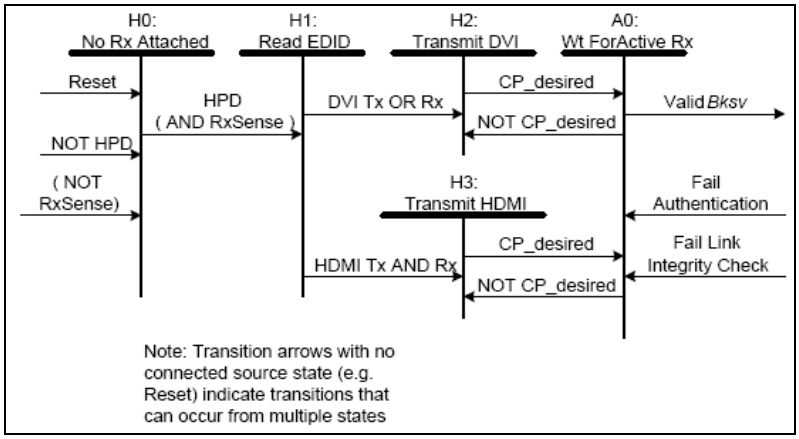

Figure 3: HDCP Transmitter Link State

Two control signals, CONTROL_A and CONTROL_B, are implemented in the PI3HDMI1210-A sink reference schematic. After changing port of PI3HDMI1210-A, CONTROL_x of the selected port sends out a >100ms pulse to reset the HPD pin of the selected port so as to reset HDCP Transmitter Link State back to H0. The relationships among SELECT, CONTROL_A/B and HPD_A/B are described below.

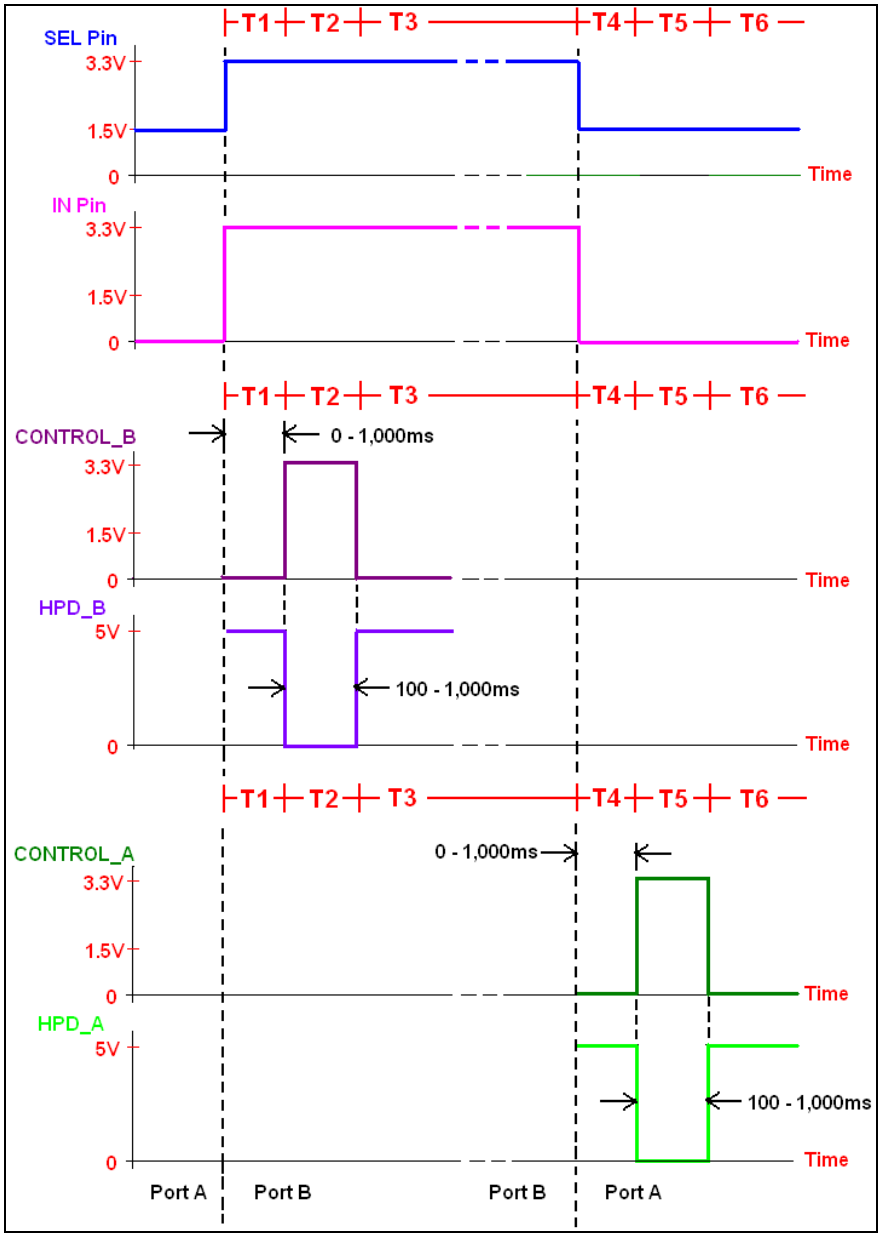

Figure 4: HDCP Control Pin Relationship

When switching from Port A to Port B by changing SEL and IN pins of PI3HDMI1210-A from low to high, it is recommended that, within 1,000ms delay (T1 shown in the figure above), a positive pulse is generated by CONTROL_B to deliver a negative pulse to HPD_B.

This negative pulse has to be at least 100ms, as specified in Chapter 8.5 of HDMI Specification Ver.1.4. The maximum width of this pulse is recommended to be 1,000ms (T2 shown in the figure above). This pulse resets the HDCP Transmitter Link State back to initial state H0.

T3 in the figure above is the normal operating cycle for Port B of PI3HDMI1210-A. At this moment, the transmitter at Port B reads the EDID data and communicates with the receiver. After linking up through exchanging HDCP key, the transmitter delivers digital audio and visual data to the receiver. When an HDCP transmitter is in normal operation, its HDCP must be sent via SCL/SDA lanes periodically with a period of no more than 2 seconds, as indicated in High-bandwidth Digital Content Protection System Specification Rev.1.4.

T4, T5 and T6 have similar performances to T1, T2 and T3, respectively, except that Port A of PI3HDMI1210-A is now selected.

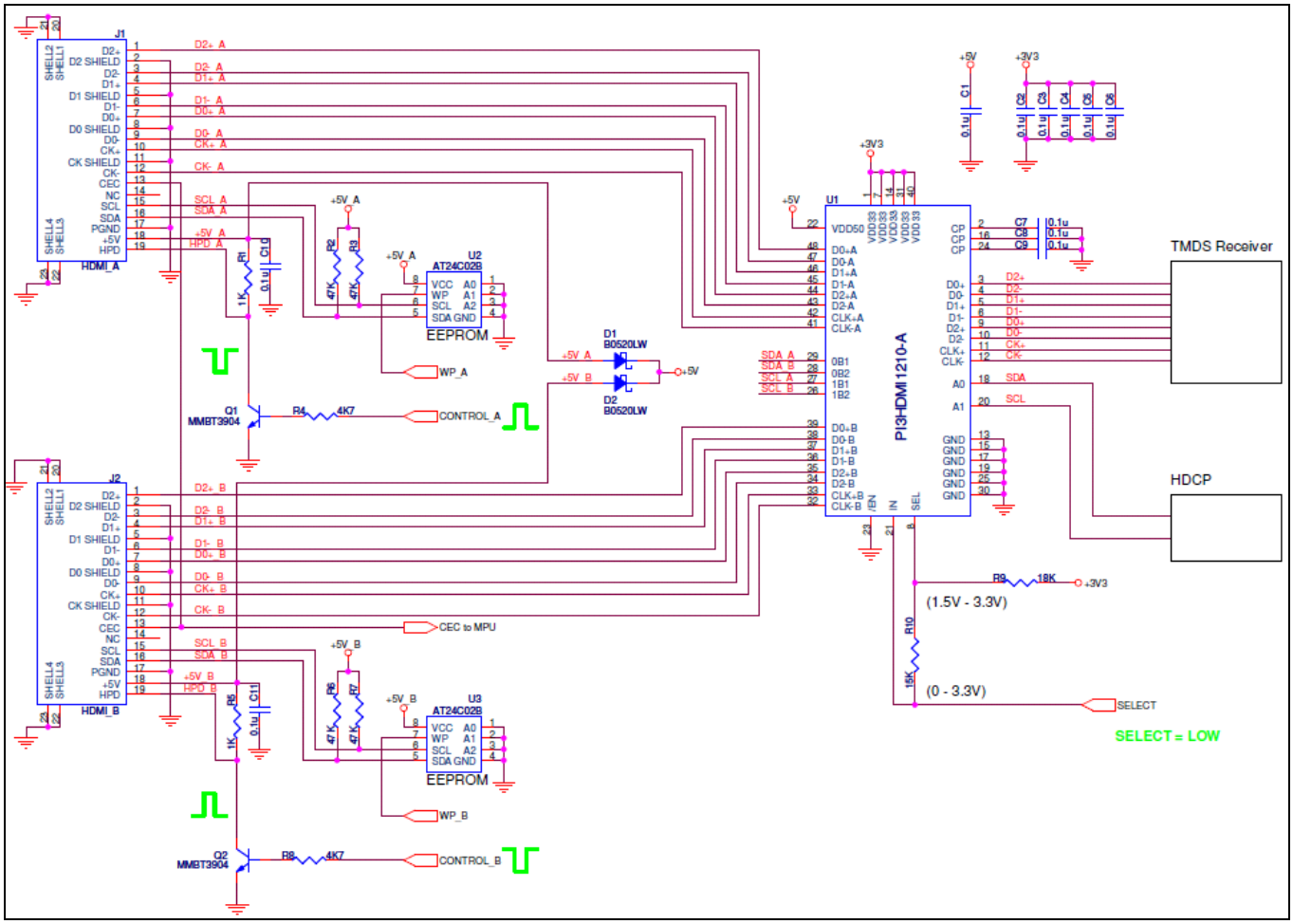

Figure 5: Port A Selection of PI3HDMI1210-A Sink Reference Schematic with HPD Reset

When both SEL and IN pins are set to a low voltage via SELECT as shown in the figure above, Port A of PI3HDMI1210-A is chosen. Differential signals will be sent from the transmitter at Port A to the receiver. The sideband signals, SDA and SCL, of Port A will be connected to HDCP of the receiver.

Conversely, if a high voltage is employed to SEL and IN pins, Port B of PI3HDMI1210-A is enabled. The differential and sideband signals will be linked between Source at Port B and Sink.

2.2 Application 2: Sink Application with HPD Reset and RxSense

Some TMDS transmitters have the ability of sensing the presence of a TMDS receiver (Receiver Sense or RxSense). Termination voltage at one pair of TMDS signals is detected by such receiver. If the signal pair goes low to indicate the absence of an HDCP receiver, the transmitter will be reset to State H0 and cease to send HDCP.

Some TMDS transmitters do not have this RxSense feature but enter long delay special mode if losing HDCP link when their port are de-selected. This special mode cannot be reset via resetting HPD, which is described in Application 1. One recommended solution is to model RxSense by removing termination at one pair of TMDS signals externally when the port is de-selected. With external RxSense circuitry implemented on TMDS clock path in the reference schematic shown above, the transmitter will enter reset state H0 and will not fall in long delay special mode.

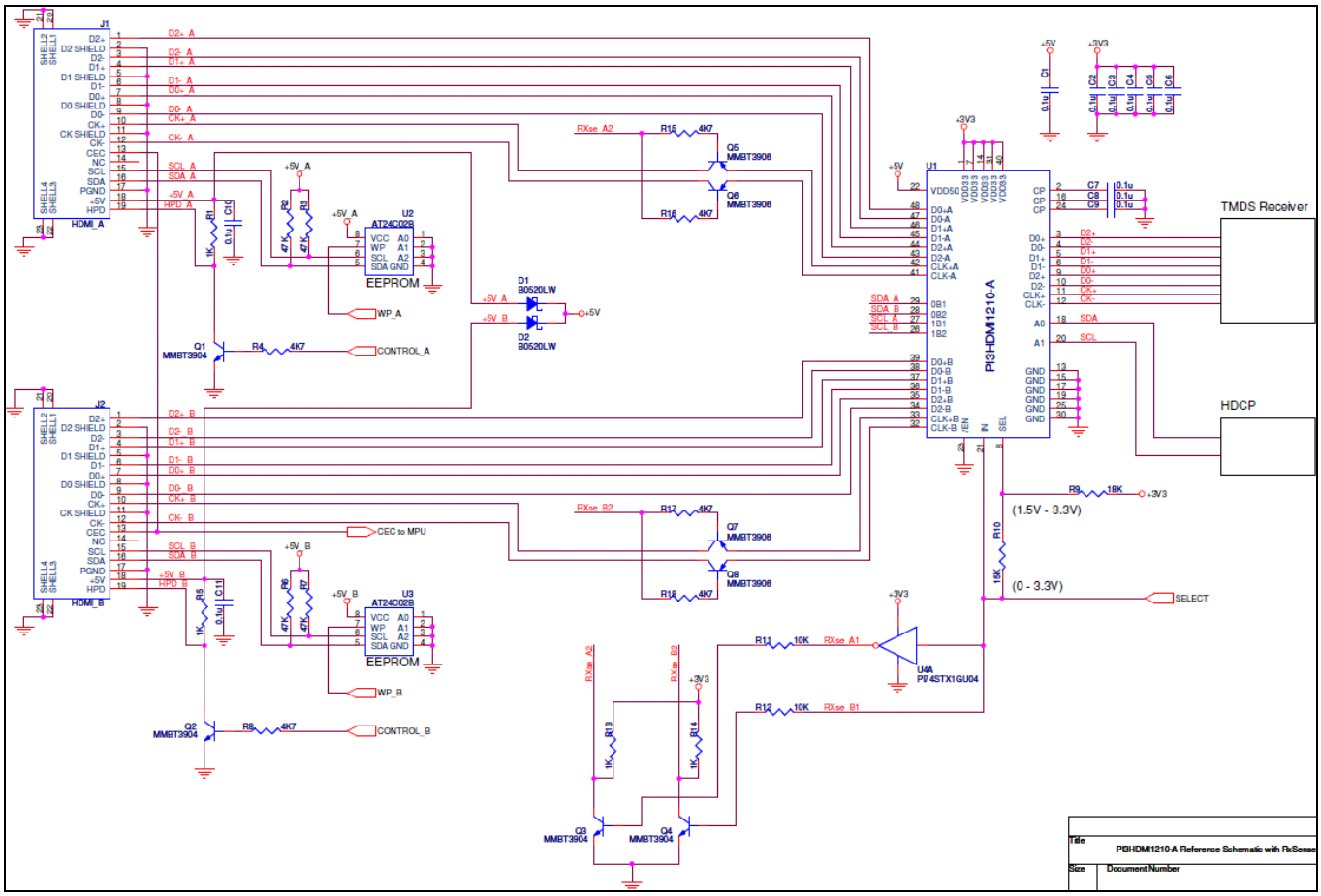

Figure 6: PI3HDMI1210-A Sink Reference Schematic with HPD Reset and RxSense

Two more control pins, RXse_A1 and RXse_B1 are added in the PI3HDMI1210-A sink reference schematic above to control RxSense circuits at Ports A and B, respectively. RXse_B1 is the same as IN pin while RXse_A1 is the inverse of IN or RXse_B1. Only one transmitter can communicate with the receiver at a time and the one not being selected is reset to state H0. The relationship between SELECT and RxSense are shown in the figure below.

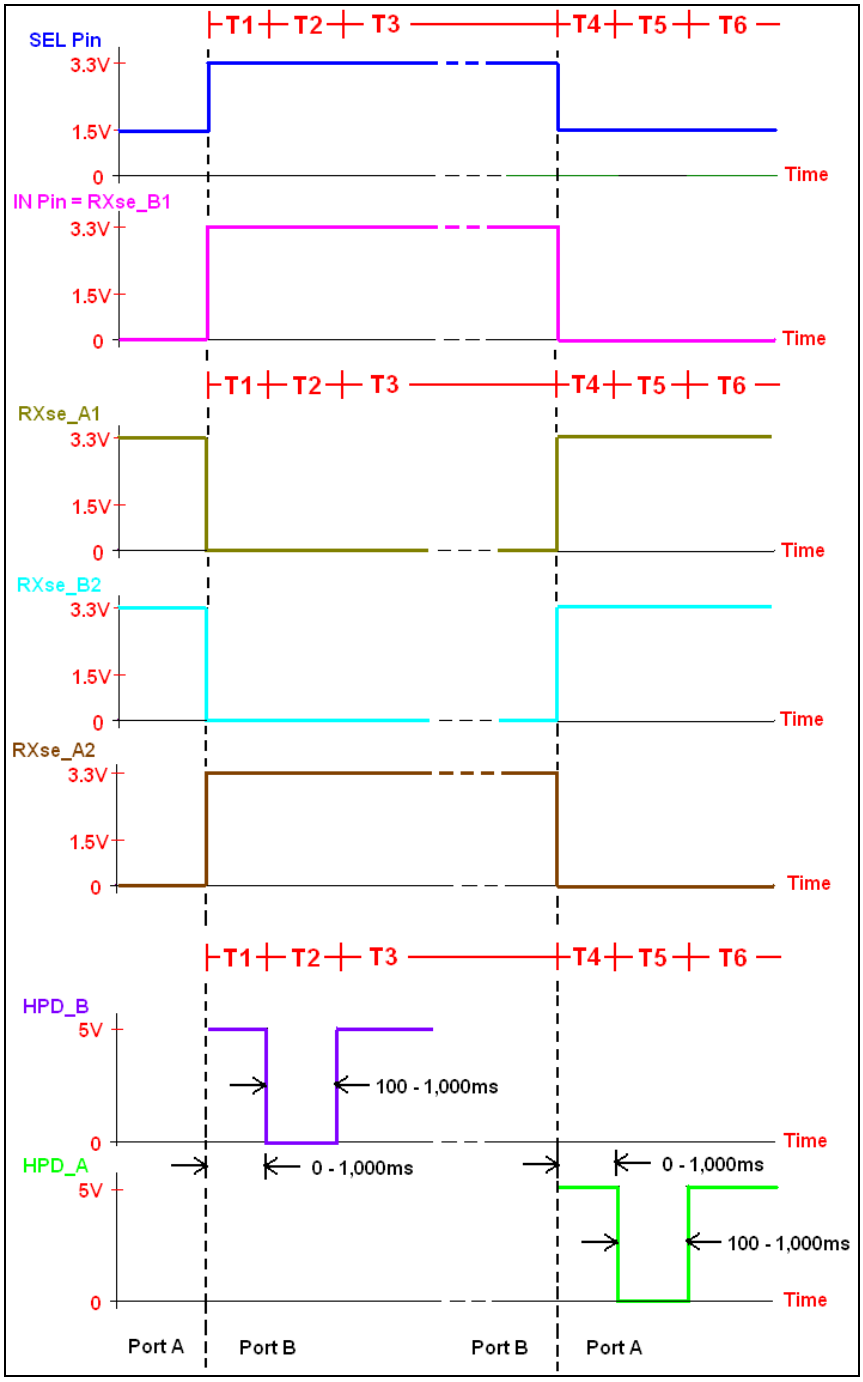

Figure 7: RxSense Conrol Pin Relationship

Port B is selected when SEL and IN pins of PI3HDMI1210-A are switched from low to high (T1 shown in the figure above). RXse_B1 and Rxse_A1 are switched to high and low, respectively. Since RXse_B1 is tied to high, the npn transistor Q4 will be closed to pull RXse_B2 to low. The pnp transistors Q7 and Q8 will result in closing the connections of CLK+/- between HDMI_B connector and PI3HDMI1210-A. Conversely, RXse_A2 is pulled up to 3.3V by +3V3 as the npn transistor Q3 is open. The 3.3V RXse_A2 will turn the pnp transistors Q5 and Q6 off. RxSense is therefore removed at Port A and transmitter at Port A is reset to initial state H0.

Within 1,000ms, the HPD_B is reset by a >100ms pulse in T2 shown in the figure 9 above. Please refer to Figure 4 for detailed functionality of HPD.

As HPD_B goes back to high in T3 in the figure above, the transmitter at Port B reads the EDID data and begins to deliver digital audio and video contents to the receiver. RXse_B1 remains high as long as the transmitter port is not changed.

T4, T5 and T6 have similar performances to T1, T2 and T3, respectively, except that Port A of PI3HDMI1210-A is now selected.

3 TDR Measurement with and without pnp Transistors

With the use of two transistors on TMDS CLK path to PI3HDMI1210-A, the TDR at TMDS CLK of the reference schematics with and without RxSense circuitry are tested. The measurement is to confirm that TDR of CLK+/- meets the sink impedance requirement even if pnp transistors are added in the PCB design. The requirement is stated in Test ID 8-8 in HDMI Compliance Test Specification Ver.1.4a.

Test ID 8-8: TMDS – Differential Impedance

Reference	Requirement
[HDMI: Table 4-20] HDMI Sink Impedance at TP2	Through-connection impedance : 100Ω ± 15%* * *A single excursion is permitted out to a max/min of 100 ohms ±25% and of a duration less than 250psecs.* At Termination impedance (when Vicm is within Vicm1 range) 100 ohms ±10%

Table 1: HDMI CTS Test ID 8-8 Specification

The data are summarized in Table 2.

Parameter		Reference Schematic Without pnp Transistors	Reference Schematic With pnp Transistors	Min Spec	Max Spec	Units
Thru	Min	96	100	85	115	Ω
Impedance	Max	112	117 (1)	85	115	Ω

Note: (1) A single excursion which is less than 250ps passes TDR requirement.

Table 2: TDR with and without pnp Transistors

Figure 8: TDR Plot at CLK without pnp Transistors

Figure 9: TDR Plot at CLK with pnp Transistors

4 References

(1) VESA DisplayPort Standard Version 1 Revision 2, Video Electronics Standards Association, January 5, 2010
(2) VESA DisplayPort Dual-Mode Standard Version 1, Video Electronics Standards Association, February 10, 2012
(3) VESA DisplayPort Interoperability Guideline Version 1.1a, Video Electronics Standards Association, February 5, 2009
(4) High-Definition Multimedia Interface Specification Version 1.4, HDMI Licensing, LLC, June 5, 2009
(5) High-Definition Multimedia Interface Compliance Test Specification Version 1.4a, HDMI Licensing LLC, March 4, 2010
(6) High-bandwidth Digital Content Protection System Revision 1.4, Digital Content Protection LLC, July 8, 2009
(7) PCI Express Board Design Guidelines Draft, Intel Corporation, June 2003