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LATCH UP TEST REPORT

Company ：**Fremont Micro Devices Co., LTD.**

Address ：**#5-8, 10-F, Changhong Science and Technology Building, Ke Ji Nan 12 Road, Nanshan District, Shenzhen, PRC**

Model Name ：**FT24C256A-UXX**

Date Received ：May 27, 2010

Date Tested ：May 27, 2010

TESTING LABORATORY IS ACCREDITED BY:

IEC/IECQ 17025 certificate of independent test laboratory approval

Certificate No.：T1117-1

ISO 9001 certificate is approved by TUV CERT certification body of TUV NORD Cert GmbH

WE HEREBY CERTIFY THAT:

The test(s) shown in the attachment were conducted according to the indicating procedures. We assume full responsibility for the accuracy and completeness of these tests and vouch for the qualifications of all personnel performing them.

	Name	Signature	Date
Testing Engineer	Jianbo Song	Jianbo Song	2010/5/27
Approving Manager	Alston Wang	Alston Wang	2010/5/27
Vice President	Coming Chen	Coming Chen	2010/5/27

Note：

1. This report will be invalid if reproduced in whole or in part.
2. This report refers only to the specimen(s) submitted to test, and is invalid if used separately.
3. This report is ONLY valid with the examination seal and signature of this institute.
4. The tested specimen(s) will only be preserved for thirty days from the date issued, if not collected by the applicant.

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1. GENERAL INFORMATION

1.1 DESCRIPTION OF UNIT

MANUFACTURER	：Fremont Micro Devices Co., LTD.
DEVICE NAME	：FT24C256A-UXX
PACKAGED / PIN COUNT	：DIP8
REFERENCE DOCUMENT	：JEDEC STANDARD NO.78B DECEMBER 2008
TRIGGER CURRENT	：25mA ~200mA (±), Step: 25mA (±)
V SUPPLY OVER VOLTAGE TEST	：5.0V~8.0V(+) , Step: 1.0V(+)
TEST TEMPERATURE	：ROOM TEMPERATURE
SAMPLE QUANTITY	：3 pcs
FAILURE CRITERIA	：If absolute Inom is < 25 mA, then absolute Inom + 10mA is used; Or If absolute Inom is > 25 mA, then > 1.4X absolute Inom is used;

2. LATCH UP TEST

2.1 TEST EQUIPMENT

Test Equipment	Equipment S/N	Calibration Date:	Recommended Due Date:
KEYTEK ZAPMASTER 7/4	0008189	May 29, 2009	May 28, 2010

2.2 LABORATORY AMBIENCE CONDITION

Temperature：23±5°C

Relative humidity：55%±10% (RH)

2.3 REFERENCE DOCUMENT

The test is based on JEDEC STANDARD NO.78B DECEMBER 2008

2.4 TEST CONDITION

I Trigger：25mA ~200mA (±), Step: 25mA (±)

Over Voltage Test：5.0V~8.0V(+) , Step: 1.0V(+)

2.5 SUMMARY OF TEST

Trigger Mode	Test Pin	Sample Quantity	Tested Result	I Trigger : Class Ⅰ
I Trigger (+)	I/P5.0V	3	PASS +200mA	**Temperature Classification:** CLASS Ⅰ: For Latch-up test at room temperature CLASS Ⅱ: For Latch-up test at maximum-rate ambient temperature
	I/O5.0V		PASS +200mA	
I Trigger (-)	I/P5.0V		PASS -200mA	
	I/O5.0V		PASS -200mA	
Over Volt Test V_{supply}	VCC5.0V		PASS +8.0V	

VSS: Pin4;

VCC5.0V: Pin8;

I/P5.0V: Pin1-3 6;

I/O5.0V: Pin5 7;

2.6 CONTENTS OF TEST

I Trigger (Positive)			
Tested Pin	Sample No. & Failed current (mA)		
	#L1	#L2	#L3
1	PASS	PASS	PASS
2	PASS	PASS	PASS
3	PASS	PASS	PASS
5	PASS	PASS	PASS
6	PASS	PASS	PASS
7	PASS	PASS	PASS

I Trigger (Negative)			
Tested Pin	Sample No. & Failed current (mA)		
	#L1	#L2	#L3
1	PASS	PASS	PASS
2	PASS	PASS	PASS
3	PASS	PASS	PASS
5	PASS	PASS	PASS
6	PASS	PASS	PASS
7	PASS	PASS	PASS

Over Voltage Test for V_{supply}			
Tested Pin	Sample No. & Failed Volt (V)		
	#L1	#L2	#L3
8	PASS	PASS	PASS