1 Introduction

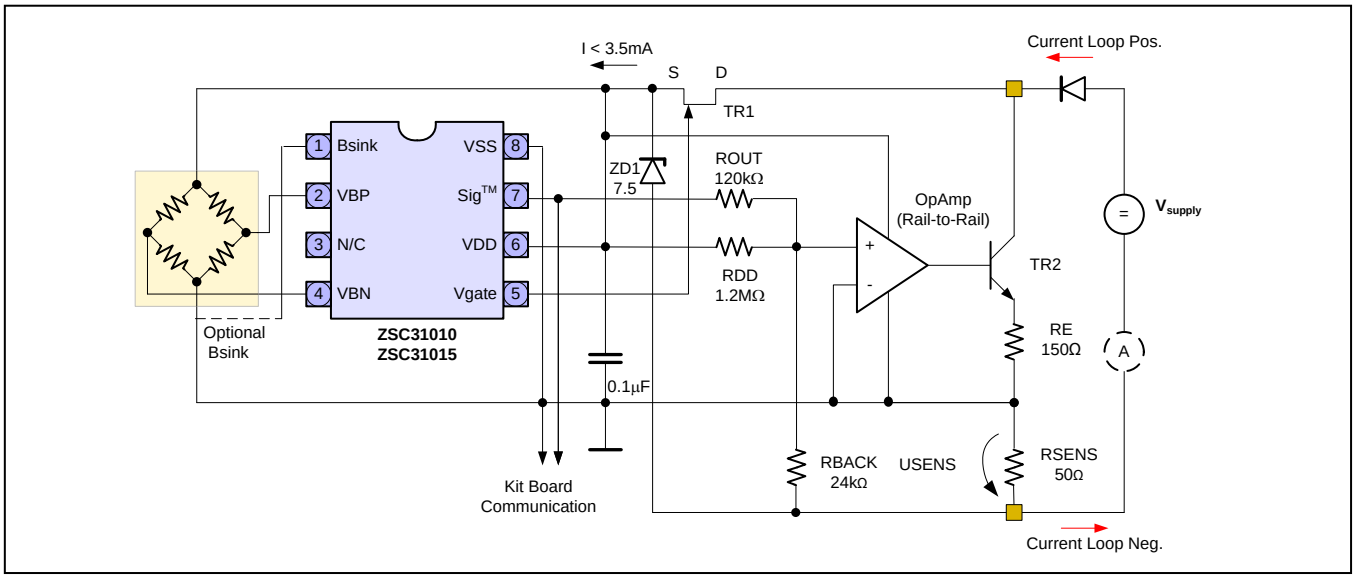
This document outlines the 4-to-20mA current loop output application for the ZSC31010/ZSC31015 SSC ICs, which are designed to interface with a resistor bridge sensor in a 3-wire sensor module. During normal operation, the Sig™/OUT pin outputs the corrected sensor reading as analog 5V ratiometric, 0 to 1V, or digital output. (During calibration/configuration, this pin acts as a bi-directional serial data channel.) The current loop output, a common robust analog output in industrial applications, was not originally supported by the ZSC31010/ZSC31015 as it is for the ZSC31050, which integrates a regulation loop that senses the actual current and regulates the output current to the calibrated target value.

Calibrating the ZSC31010/ZSC31015 for a current loop output application requires a different method of starting the Command Mode (CM) for communication. The command to enter CM must be sent within the command window, which is the first 5ms after power up for the ZSC31010 or the first 3ms for the ZSC31015. Meeting the command window requirements is especially complicated with a current loop application, particularly for the ZSC31015. The recommended method is to send the “Start CM” command before turning on the current loop voltage supply. This procedure is an exception to standard procedures: even if the absolute maximum ratings given in the data sheet are not observed, it will not harm the IC because there is no significant power consumption via the communication lines. If the master communicates via a push-pull stage, no pull-up resistor is needed; otherwise, a pull-up resistor with a value of at least 150 Ω must be connected.

2 ZSC31010/ZSC31015 with 4-to-20mA Current Loop Output

With additional external circuitry (see Figure 2.1), the calibrated voltage output signal can be transformed into a corresponding current loop output ranging from 4 to 20mA. To achieve high accuracy, an additional step is necessary to correct errors caused by the resistor tolerances of the external circuitry. The error of the analog output buffer, which is not included in the calibration path, can also be corrected.

Figure 2.1 – ZSC31010 with Current Loop Output Using ZACwire™ Communication



With the circuitry in Figure 2.1, the objective is to convert the 10% to 90% VDD output of the ZSC31010/ZSC31015 to a corresponding 4 to 20mA current loop output. To keep the output current small, RDD and ROUT must be chosen in the ratio ROUT = RDD/10 with RDD in the range of megohms. The resistor values are discussed in detail in section 3. For the op amp, a low power 5V rail-to-rail type must be used (e.g., OPA337). The Zener diode (7.5V) provides overvoltage protection for the VDD line. TR1 is an N-channel type JFET as recommended in the data sheets (e.g., BSS169 or DN3545). For TR2, an NPN transistor with a power consumption rated for the actual supply voltage must be selected (e.g. BCX56 or FZT651).

Important: The voltage supply and the amp meter of the current loop must be galvanically separated from the PC / Kit Board ground.

3 Current-Loop Calibration

The following special calibration procedures required for this application use the same calibration steps as for the voltage output mode but include an additional calibration step to change the target values VOUT/VDD [%], (named Measure [%] in the software) in the calibration procedure to correct the errors.

Step1

Separately determine the additional error of the external circuitry and the back end with a two-point current measurement versus the DSP DAC control.

Step2

Use a formula with offset and gain errors to calculate the new target values “Measure [%].”

Step3

Use the new values in the ZSC31010/ZSC31015 calibration window and calculate the coefficients in the same way as for the voltage output mode.

The loop current is determined by the following transfer function for the current loop current $I_{CL}=f(V_{OUT})$.

$$\boldsymbol{I_{CL}}=U_{SENS}/R_{SENS}=(R_{BACK}*V_{DD})/(100*R_{SENS}*R_{OUT}) * \boldsymbol{V_{OUT}/V_{DD}} + R_{BACK}*V_{DD}/(R_{SENS}*R_{DD}) \qquad \textbf{Equation 1}$$

With

$$Gain = (RBACK*VDD)/(100*RSENS*ROUT) \qquad \textbf{Equation 2.1}$$

$$Offset = RBACK*VDD/(RSENS*RDD) \qquad \textbf{Equation 2.2}$$

The current can be calculated as

$$I_{CL} = Gain * V_{DAC}[\%] + Offset \qquad \textbf{Equation 3}$$

The 11-bit (12-bit) output DAC of ZSC31010/ZSC31015 is controlled by the DSP and uses the normalized value.

$$V_{DAC}\ [dec]=ROUND(target\ value[\%]*2^{14},0) \qquad \textbf{Equation 4.1}$$

The 4-digit hex code is calculated

$XXYY = DEC2HEX(V_{DAC}\,[dec],4)$ **Equation 4**

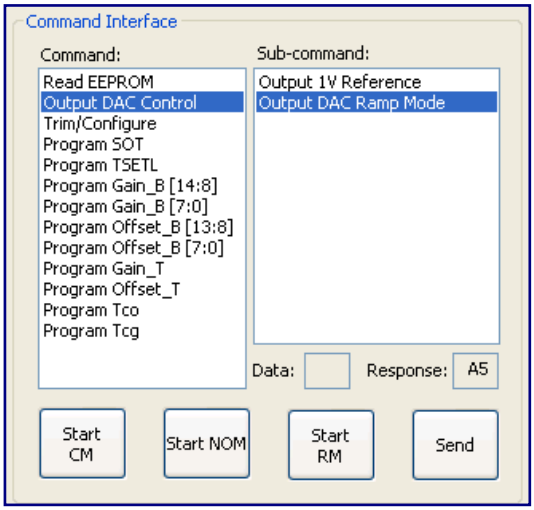
For example (V_{DD}=5.000V):

For the target value of 10%, $V_{OUT}/V_{DD} \rightarrow V_{DAC} = 1638_{dec} \rightarrow XXYY = 666_{hex.}$ **Equation 5.1**

For the target value of 90%, $V_{OUT}/V_{DD} \rightarrow V_{DAC} = 14746_{dec} \rightarrow XXYY = 399A_{hex}$ **Equation 5.2**

The DAC is controlled by writing the XXYY value in the Gain_B EEPROM bits <51:44> for the ZSC31010 or <31:17> for the ZSC31015. Offset_B must be set to 0x00. The output mode must be set to ratiometric, and the JFET regulation must be set to 5V. All other settings do not matter for this test. The necessary control command *0x205X* (*ZSC31010/ZSC31015**)*** is sent by the Evaluation Kit software. Send the “Start CM” and connect the Vsupply.

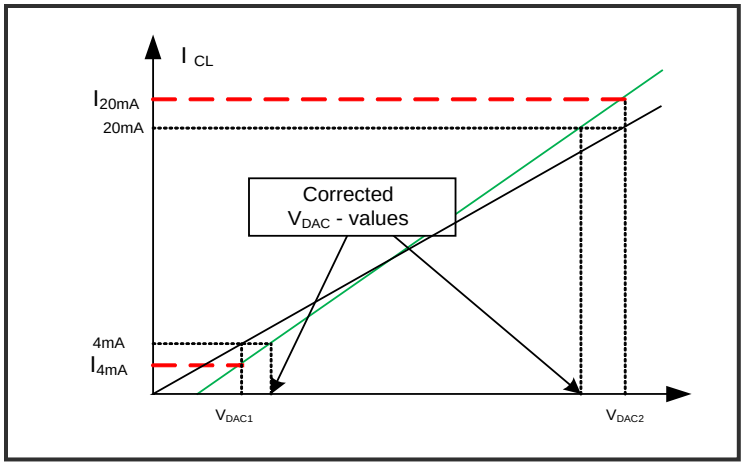
Figure 3.1 Sending the DAC Command



- Start Command Mode
- Program Gain_B [14:8] XX --> SEND
- Program Gain_B [7:0] YY --> SEND
- Program/Keep Offset_B 00 (step size 0)
- Output DAC Control --> Output DAC Ramp Mode
- Measure I_{CL}

Figure 3.2 illustrates the method for calculating these corrected target values. The blue line shows the ideal function described by equation 2. The green one is the error-line (with 2 current measurement points).

Figure 3.2 Line Correction



This transfer function for the measured currents I_{4mA} and I_{20mA} is given by

$$I_{xmA}=(Gain+\Delta Gain) * V_{out}/V_{DD} + (Offset+\Delta Offset) \quad \textbf{Equation 6}$$

With the selected resistor values (Figure 2.1), RSENS=50Ω, RDD=1.2MΩ, ROUT=120kΩ, RBACK=24kΩ, and the recommended IC supply voltage VDD = 5V, Gain = 0.2mA, and Offset = 2mA.

The “error-free” target values

$$V_{out}/V_{DD} = (I_{CL\_min} -2mA)/0.2mA = 10\% \text{ corresponds with } I_{CL\_min}=4mA \quad \textbf{Equation 7.1}$$

$$V_{out}/V_{DD} = (I_{CL\_max} -2mA)/0.2mA = 90\% \text{ corresponds with } I_{CL\_max}=20mA \quad \textbf{Equation 7.2}$$

The offset and tolerances of the circuitry cause different values of ICL when setting the DAC to these values. After the DAC has been set to the corresponding values (666_{hex}, $399A_{hex}$), the resulting currents I_{4mA} and I_{20mA} must be measured to determine the error values ΔGain and ΔOffset.

$$\Delta Gain = (I_{20mA} – I_{4mA})/(V_{DAC2}-V_{DAC1})- Gain \quad \textbf{Equation 8.1}$$

$$\Delta Offset =I_{4mA}-(Gain+ \Delta Gain)*V_{DAC1}- Offset \quad \textbf{Equation 8.2}$$

These equations can be used to re-calculate the target values:

$$V_{DAC\_4mA} = 4 \text{ mA} * (2mA + \Delta Offset)/(0.2mA +\Delta Gain) \quad \textbf{Equation 9.1}$$

$$V_{DAC\_20mA} = 20 \text{ mA} * (2mA + \Delta Offset)/(0.2mA +\Delta Gain) \quad \textbf{Equation 9.2}$$

This calculation can be done with Excel™ sheet *ZSC31010_ZSC31015 Current Loop Calibration.xls*. Software support is pending.

The Excel™ sheet also allows re-calculating the DAC control values in case different resistor values are selected.

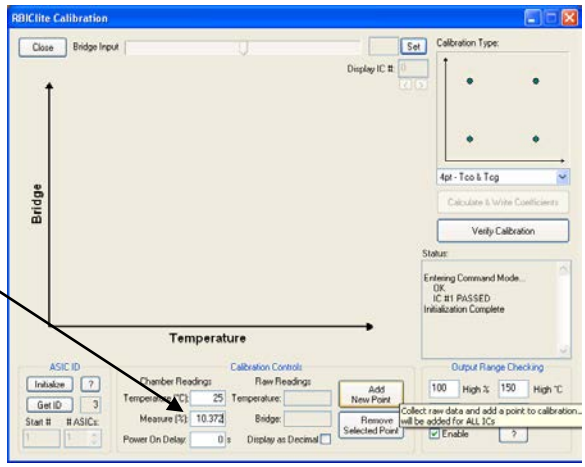
4 Example

The measured currents I_{CL4mA} =3.926mA (for Gain_B=0x666 in DAC Ramp Mode) results in 10.327% instead of the original 10% and I_{CL20mA} =19.823mA (for Gain_B=0x399A in DAC Ramp Mode) results in 90.891% instead of the original 90%.

Using the common calibration window, the calculated value must now be used for calibration as shown in Figure 4.1.

Figure 4.1 Calibration with Corrected Target Values Measure[%]

	A	B	C	D	E	F
1						
2	**Calibration-Correction for Currentloop mode**					
3						
4		V_{DD}[V]	R_{out}[Ohm]	R_{DD}[Ohm]	R_{back}[Ohm]	R_{SENS}[Ohm]
5		5.000	1.20E+05	1.20E+06	2.40E+04	50
6						
7	Input:	V_{DAC}/V_{DD} [%]		Current values(mA)	V_{DAC}/V_{DD} corrected[%]	
8	Pmin	10.000	I1	4.000	10.372	
9	Pmid(SOT_Bridge)		I2			
10	Pmax	90.000	I3	20.000	90.891	
11						
12						
13						Gain [A]
14						Offset [A]
15	First measure point:		I_{4mA}[mA]	3.926	mA	ΔGain
16	Second measure point:		I_{20mA}[mA]	19.823	mA	ΔOffset
17						
18						
19						
20						



5 Related Documents

Document
ZSC31010 RBic$_{Lite}$™ Data Sheet
ZSC31015 RBic$_{dLite}$™ Data Sheet

Visit www.IDT.com/ZSC31010 and www.IDT.com/ZSC31015 or contact your nearest sales office for the latest version of these documents.

6 Definitions of Acronyms

Term	Description
CM	Command Mode
DAC	Digital-to-Digital Converter
DSP	Digital Signal Processing
SSC	Sensor Signal Conditioner

7 Document Revision History

Revision.	Date	Description
1.0	January 8, 2009	First release
1.1	February 22, 2010	Revise command window period from 1.8ms to 3.0ms for the ZSC31015.
1.2	July 28, 2010	Revised product names from ZMD31010 to ZSC31010 and from ZMD31015 to ZSC31015.
1.21	March 2, 2011	Update for contact information.
	April 19, 2016	Changed to IDT branding.

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138
www.IDT.com

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com/go/sales

Tech Support
www.IDT.com/go/support