The Differences Between MEM OS And XO

Pericom Timing Application Engineering

Introduction

MEM OS (Oscillator) is composed of MEM (micro_electro_mechanics) resonator as internal reference and conventional silicon PLL technology to generate output clock. MEM resonator needs a special silicon process and its low Q characteristics results high unbounded phase noise (high random jitter). Therefore, silicon PLL circuit (Phase Lock Loop) must be used to constrain the OS final output clock noise. Also, on-chip temperature compensation circuit is used for the cancellation of low Q temperature instability.

On the other hand, XO (crystal oscillator) directly uses crystal nature extreme high Q, stability, and reliability with relative simple active circuits, such as crystal oscillator amplifier and clock buffer driver circuits.

Due to the differences of above two manufacturing technologies of oscillator, customers ask and are concerned with the differences of applications of two technologies in the design of their systems. This application note presents the way to observe the oscillator's electrical differences through an example of 125MHz oscillator reference clock source to drive 1GE(Giga Bit Ethernet) Serdes (Serializer/deserializer pair). The results are shown by testing the data link eye jitter differences since Serdes BER (Bit Error Rate) is directly related with the RX input eye opening in margin. In the extreme case, 1UI (Data Unit Interval) peak-peak eye jitter makes the transmission eye fully closed, and, consequently, data transmission is then broken. Other than <1UI data eye jitter on certain bits correspond to the certain BER as shown in Figure 1. In other words, different systems (Serdes ASIC, reference clock , and channel length, etc.) all have their own bathtub curve shape corresponding the eye opening for that data stream.

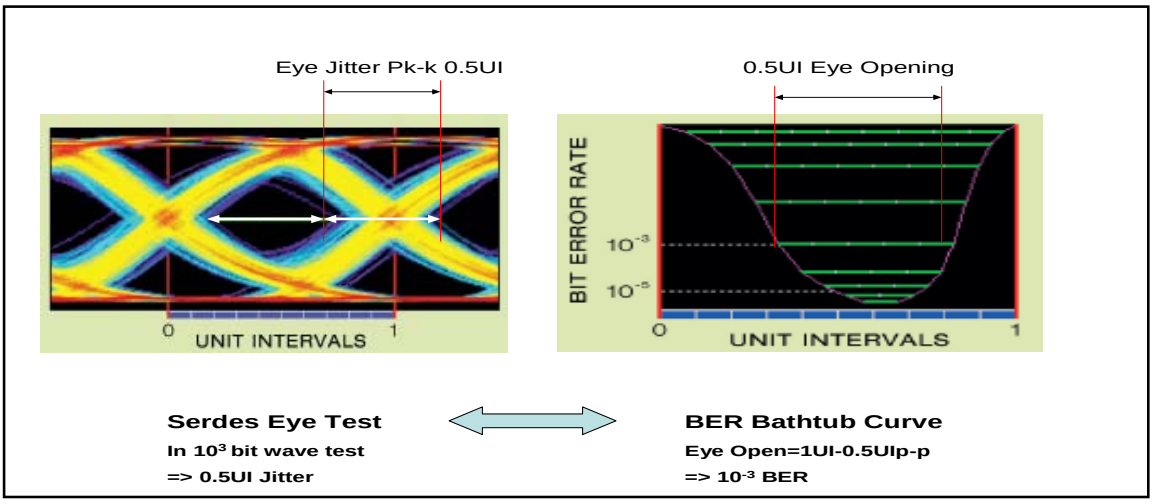


Figure 1: Eye jitter and bathtub curve relation with BER

General Serdes System Model

1) Serdes Model Components

As shown in Figure 2, Serdes TX PLL directly uses reference clock to generate the output data rate stream. For example, 1 Gb/s Ethernet has the max. equivalent data stream clock of 625MHz which is generated from 125MHz reference clock. In other words, reference clock jitter directly results in TX eye jitter through TX PLL, which is dependent on the PLL bandwidth and its own circuit characteristics. Considering RX PLL bandwidth, the final Serdes reference clock jitter transfer function is a band-pass function and with peaking in Figure 3 red line.

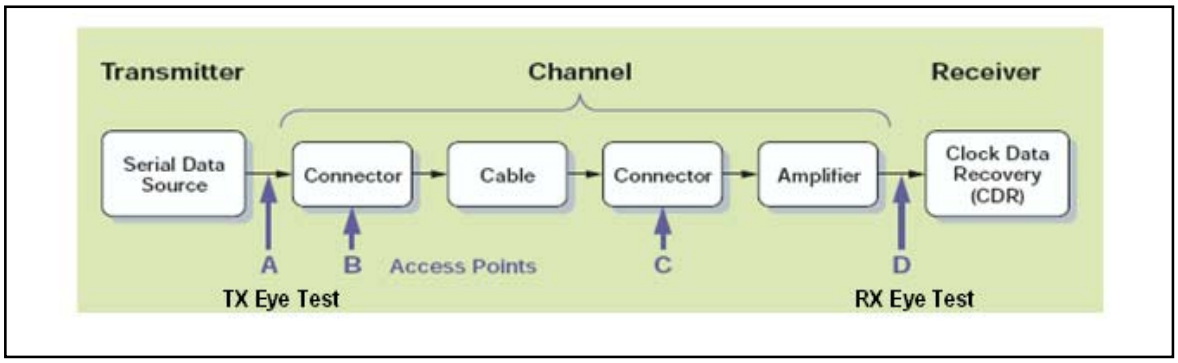


Figure 2: Serdes data Transmission model

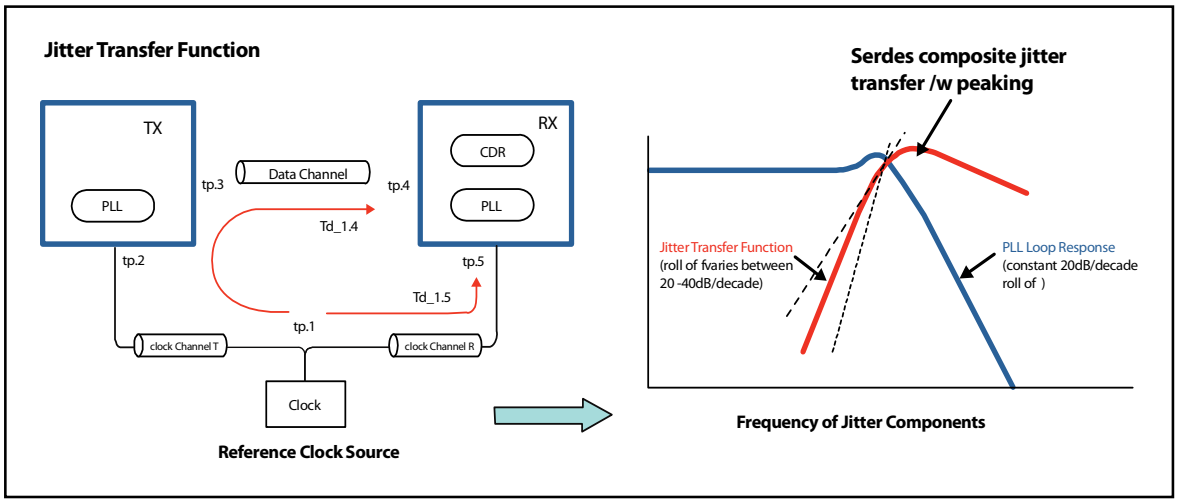


Figure 3: Serdes model ref. clock jitter transfer function

It is worth to note that random jitter's characteristic is that all source jitters will finally supper add on each other with time and data packets count. For example, reference clock random jitter, TX PLL self random jitter, and group delay jitter on transmit channel are all supper added in statistical manner on the final eye jitter. The following example demonstrates the detailed working of how the different reference clock sources (XO vs. MEM OS) jitter reflect on the two kinds of Serdes transmission models: 1R (one Serdes re-timing) in Figure 4. and 2R with 30in PCB trace in Figure 5.

2) 1R Serdes Model In Different Oscillators

In Figure 4, Serdes TX PLL directly uses reference clock to generate the output data 1Gb/s stream. For example, 1 GE has the max. data stream clock frequency of 625MHz generated from 125MHz reference clock. Applying MEM OS or XO in the same platform can tell what the difference of data eye jitter is.

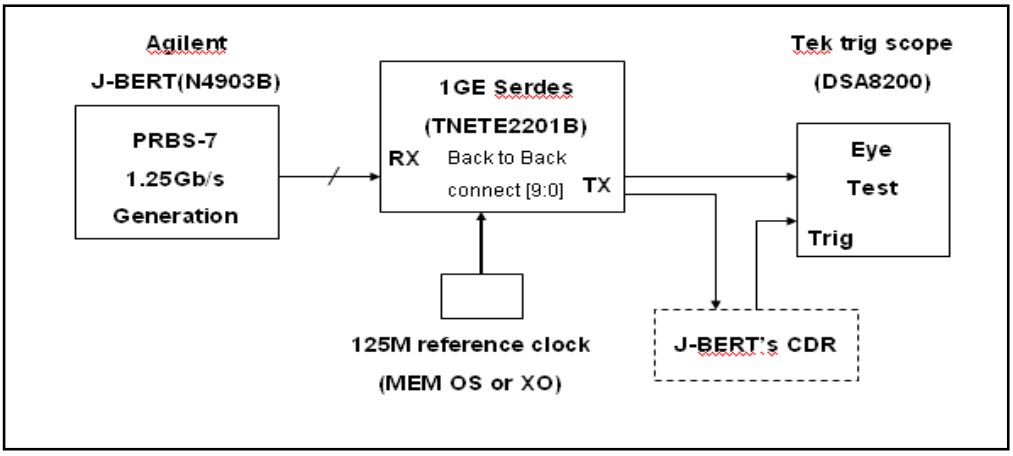


Figure 4: 1R Serdes model in different oscillators

3) 2R Serdes Model In Different Oscillators

Figure 5 shows two sets of 1R Serdes models, which use two reference clocks of the same kind at the same time to re-time the data stream. In addition, 30-in PCB trace is inserted to generate some transmission line data dependent jitter, which is random since the data stream is PRBS-7 pseudo random pattern for the real data emulation.

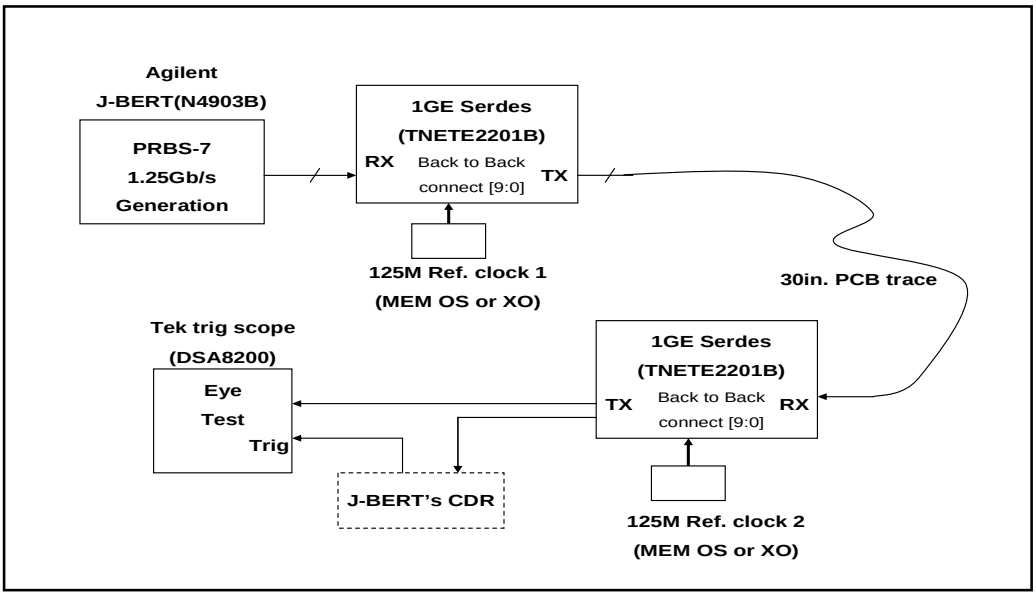
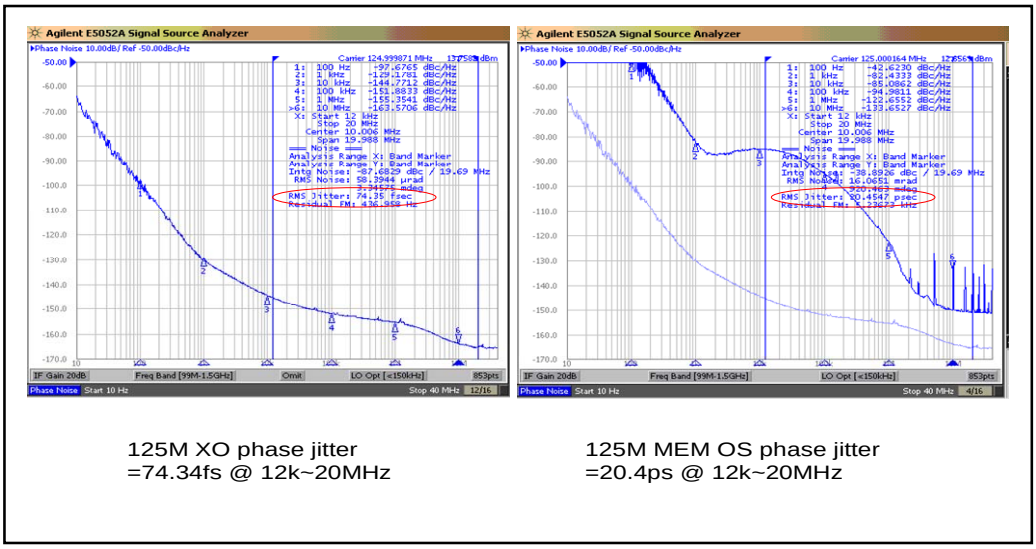


Figure 5: 2R Serdes model in different oscillators

How to Tell Jitter Differences in MEM OS and XO?

A) MEM OS vs. XO Characterization Jitter Difference

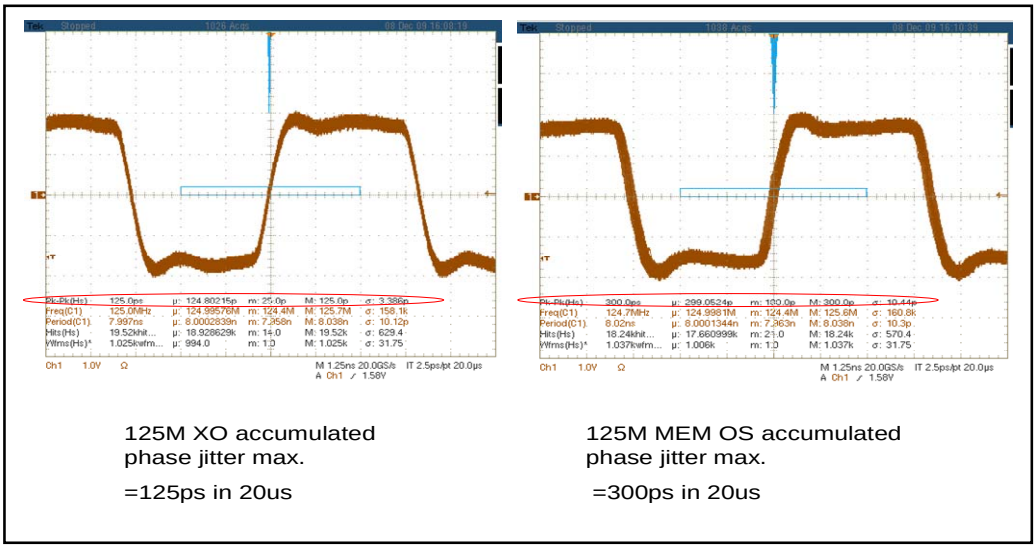
With Agilent source signal analyzer E5052A and Tek scope TDS7404 to measure phase noise RMS jitter and time accumulated jitter, MEM OS shows significantly worse (>250times) phase noise integrated RMS jitter than XO in Figure 6. Meanwhile, MEM OS shows 140% larger scope accumulated jitter than XO under 20us accumulation delay and 1k waveforms test, which is 300ps vs. 125ps in Figure 7.



125M XO phase jitter
=74.34fs @ 12k~20MHz

125M MEM OS phase jitter
=20.4ps @ 12k~20MHz

Figure 6: 125MHz XO vs. MEM OS phase jitter at 12kHz-20MHz: 0.074ps vs. 20.4ps



125M XO accumulated phase jitter max.

=125ps in 20us

125M MEM OS accumulated phase jitter max.

=300ps in 20us

Figure 7: 125MHz XO vs. MEM OS scope 20us accumulated jitter: 125ps vs. 300ps

B) 1R and 2R Serdes Data Jitter in MEM OS vs. XO

In 1R Serdes model with 125M MEM OS vs. XO reference clock without PCB trace, the Serdes data eye jitter measured in MEM OS is 13.8% worse than XO as reference clock as observed in Figure 8. But, in 2R Serdes model, when two MEM OSs are used with the additional 30-in PCB trace, the 2nd stage Serdes output data eye jitter becomes 30% worse than that in the model where 2 XOs are used in 30k acquisition eye test as in Figure 9,. It can be predicted that as more MEM OSs are used in more Serdes system and longer PCB trace or longer transmission line generating higher data stream group delay jitter is used, the final RX end data jitter is dramatically worse than the model that uses all XOs.

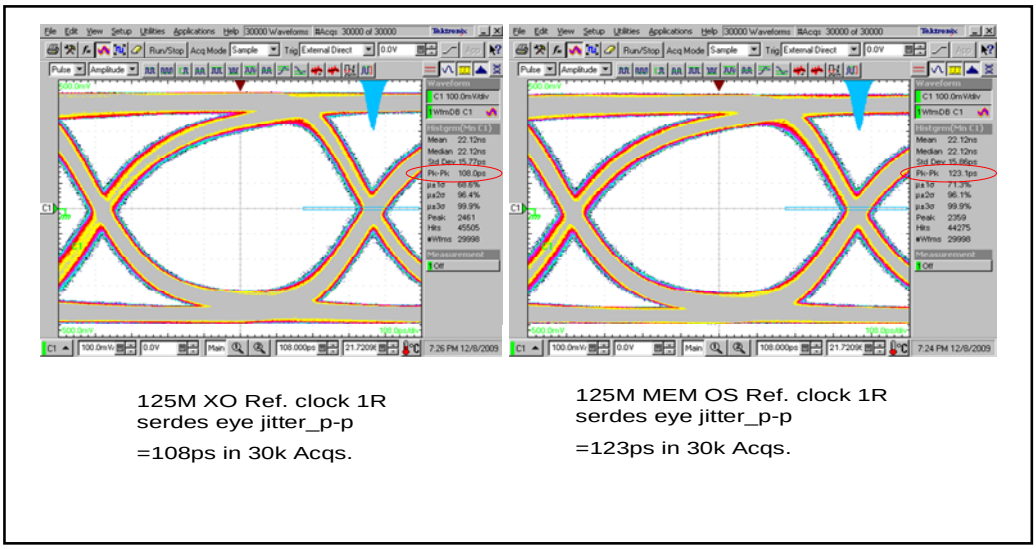


Figure 8. 1R serdes model data eye jitter in XO vs. MEM OS: 108ps vs 123ps

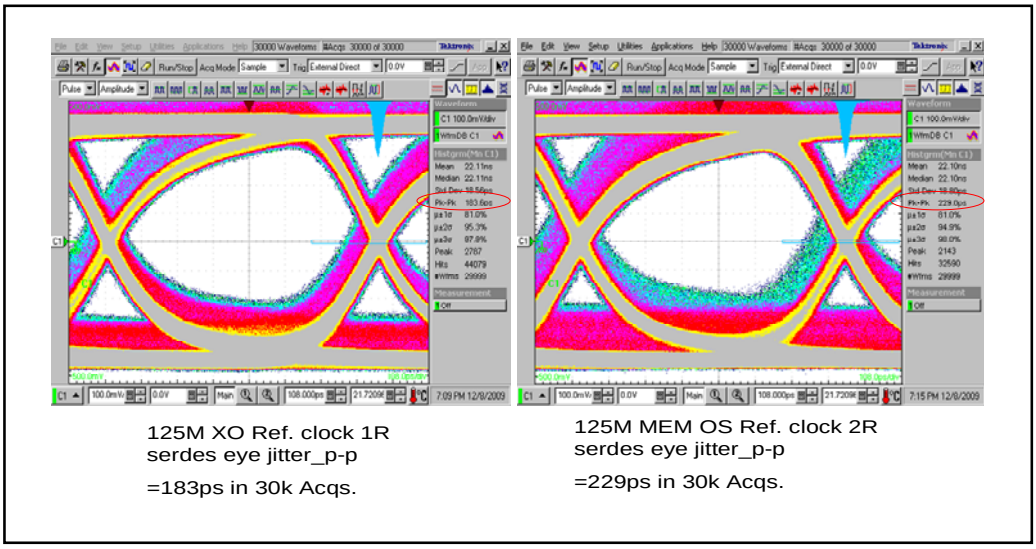


Figure 9. 2R serdes model data eye jitter in XO vs. MEM OS: 108ps vs 123ps

Conclusion

MEM OS is a newer oscillator technology in FCP (Frequency Control Products) industry, compared to the long time proven XO technology. MEM OS's intrinsic high random jitter, especially in the clock close-in phase noise, causes more Serdes link data jitter penalty than that of general XO. This penalty results in long term reliability and compliance issues in the end products, such as incompatibility with other devices or higher data failure rate in the system between different vendor products.

As more MEM OSs, the longer PCB trace or longer transmission line (higher data stream group delay jitter), and the other longer logic delay in synchronous system design are used in the system, the system shows more jitter difference than that of the system using XOs. This is because that MEM OS clock high jitter is unbounded random jitter, which is supper added on all random jitter sources in the system. This situation gets worse in high bit-rate Serdes systems since its eye UI absolute time is getting much shorter and jitter tolerance time is much smaller accordingly. For example, 1.25Gb/s 0.5UI jitter tolerance is 400ps, but XAUI 3.125Gb/s with the same 0.5UI jitter tolerance is only left 80ps. Customer are strongly advised to fully perform system test in all respects before applying MEM OSs in their system integration design.

Contact Information

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References

1. Pericom application note #218 "Pericom PCIE 1.0 and 2.0 Advanced Clock Solutions"
2. Jon Titus, "It's Crystal Clear: Quartz Still Resonates with Designers", ECN 2006
3. Pericom product guide " SaRonix-eCera Crystals & Oscillators" 2009
4. "Phase Noise and Jitter Requirements for Serial I/O Applications", Sitime application note

DUT Reference

1. Sitime MEM OS 5x7 CMOS 125MHz (SiT8102AC-43-33E-125.00000)
2. Pericom 5x7 CMOS 125MHz XO (FNC500006)
3. Pericom 1GE serdes EVB with TI serdes chip (TNETE2201B)