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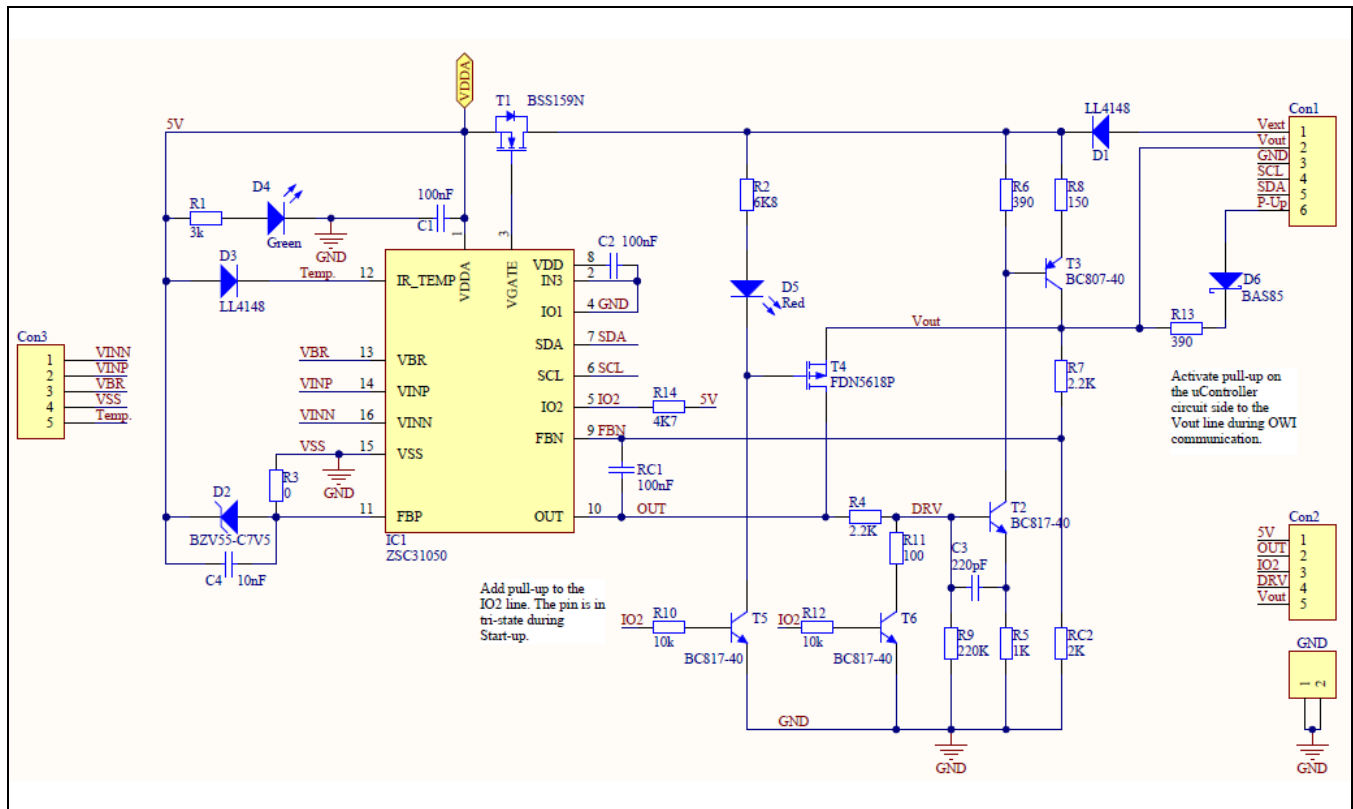
2 Application Configuration

The configuration is determined by the programming of the ZSC31050 and by the placement and value of the external parts given in the schematics in Figure 1.1 and Figure 2.1. For full details for programming and configuration of the ZSC31050 with the SSC Evaluation Kit, see the *ZSC31050 Evaluation Kit Description*.

2.1. Schematic Circuit

A three-wire solution for 0V to 10V analog output using the ZACwire™ interface can be achieved by modifications implemented in the schematic in Figure 2.1. The logic will separate the analog and digital signal paths depending on the operational mode. In the resulting circuit, the reduction in the number of connection wires achieved by adding a few components to the schematic reduces installation and maintenance costs.

Figure 2.1 Three-Wire 0V to 10V Analog Output with ZACwire™ Interface



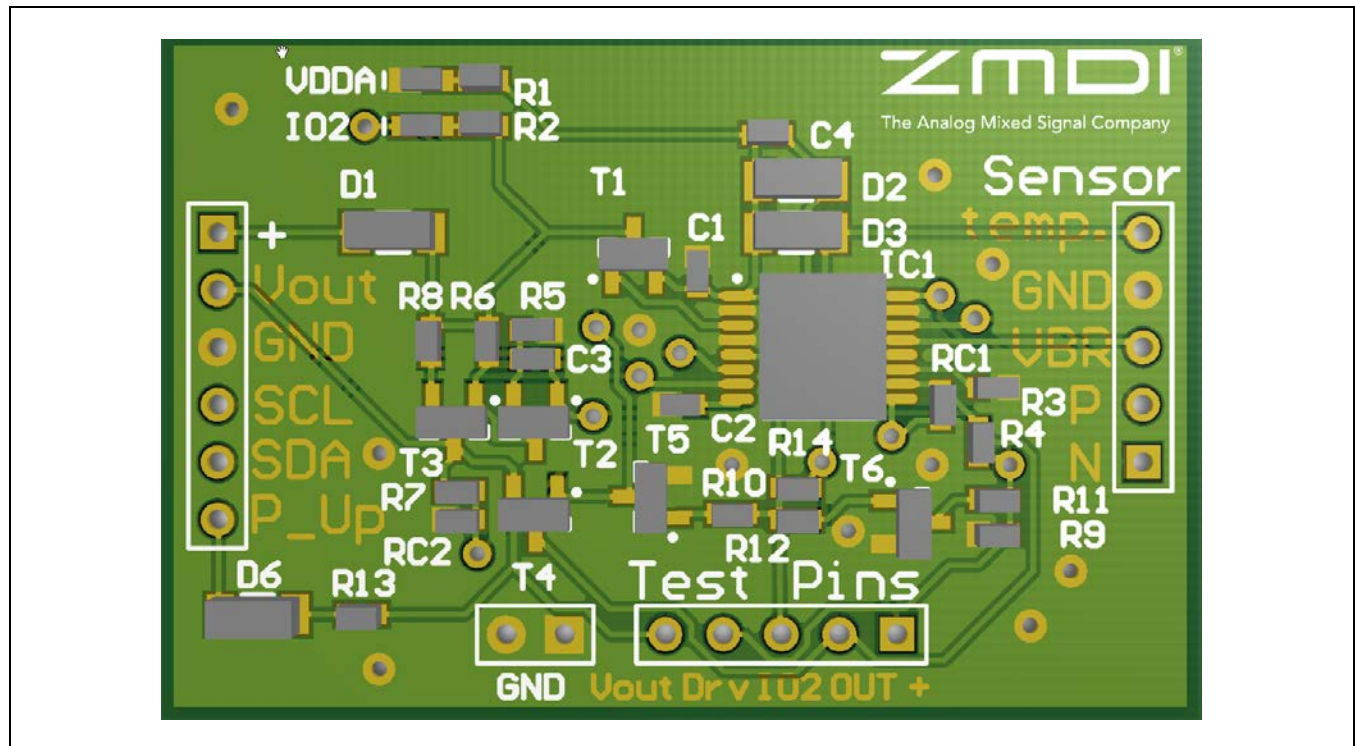
Additional configuration of the ZSC31050 is needed to ensure proper triggering of the switch. See section 2.3 for the configuration settings using the ZSC31050 SSC Evaluation Kit Software. The IO2 port mode must be enabled as ALARM2 and active HIGH (EEPROM register 1B_{HEX}), and the alarm threshold must be set to FFF9_{HEX} (EEPROM register 13_{HEX}). With these settings, the IO2 pin switches state from HIGH during the 20ms startup window to LOW when entering the Normal Operation Mode (NOM). This behavior can be used to trigger and open the communication channel for the ZACwire™ interface. Within the 20ms window, if a START_CM command is received, the communication channel stays open in Command Mode (CM); otherwise the ZSC31050 enters the Normal Operating Mode (NOM) and the analog output is active.

The addition of the T4 MOSFET ensures there will not be a high voltage signal at pin 1 (B2) of IC1 before the T2 and T3 transistors conduct. A pull-up resistor must be connected to the IO2 pin in order to achieve the logic-high level during start-up window. When programming the device, an additional pull-up must be implemented on the Vout line from the programming microcontroller (D6 and R13).

A temperature measurement can be implemented using the D3 diode.

2.2. PCB Layout

Figure 2.2 PCB Layout



An example Gerber file is available on the IDT website (see section 4).

2.3. Evaluation Software Configuration

Table 2.1 lists the register bits that must be configured to ensure proper triggering of the IC1 switch. Figure 2.3 shows the settings for these bits using the ZSC31050 SSC Evaluation Kit Software.

Figure 2.3 ZSC31050 SSC Evaluation Kit Software Configuration

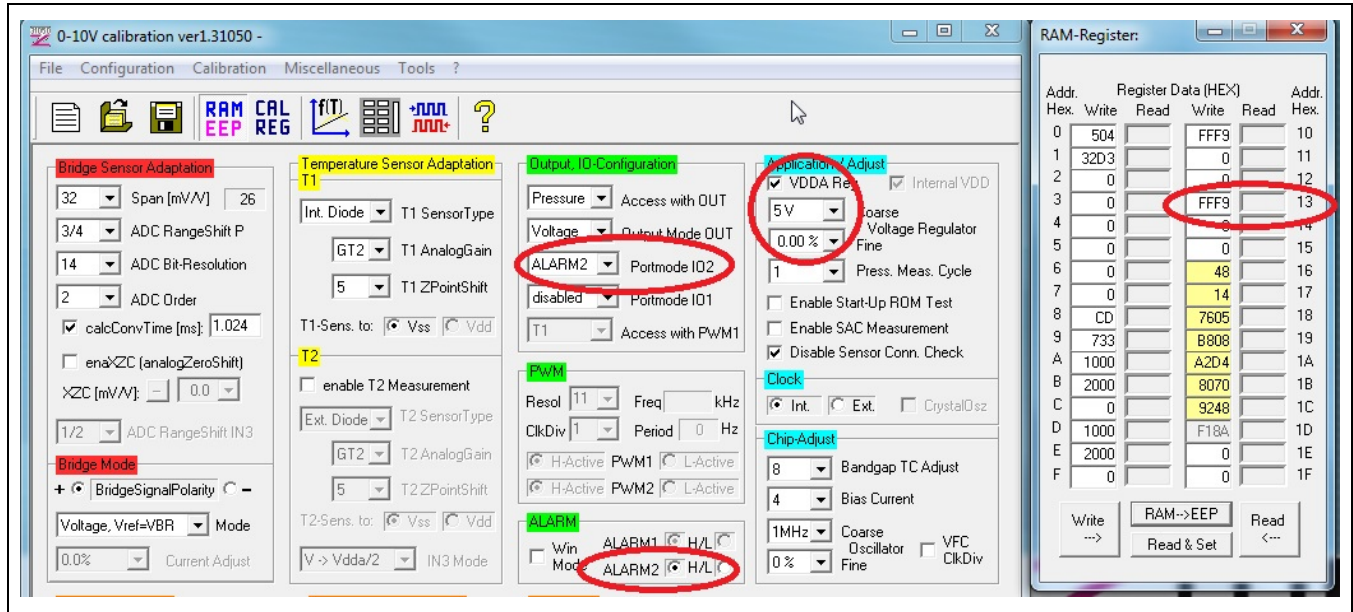


Table 2.1 Register Configuration

Settings	Register	Register Name	Bits	Comment
Port Mode IO2	1B _{HEX}	CFGOUT	4	Enable Alarm 2
Port Mode IO2	1B _{HEX}	CFGOUT	5:6	Alarm high-active
IO2 Alarm	13 _{HEX}	-	0:15	Alarm 2 threshold
Supply Voltage VDDA	18 _{HEX}	CFGAPP	1:2	Coarse regulation
Supply Voltage VDDA	1C _{HEX}	ADJREF	10:12	Fine regulation

2.4. Output Voltage Adjustment V_{OUT}

The following procedures will compensate components' parameter variations in order to achieve the desired output voltage of 0-10V.

- Calibration and coefficient calculation (initial targets: 10% and 90%)
- Analog output measurement
- Re-adjustment of target values (manual calculation via equation (2)) and limit values and calculation of the new coefficient

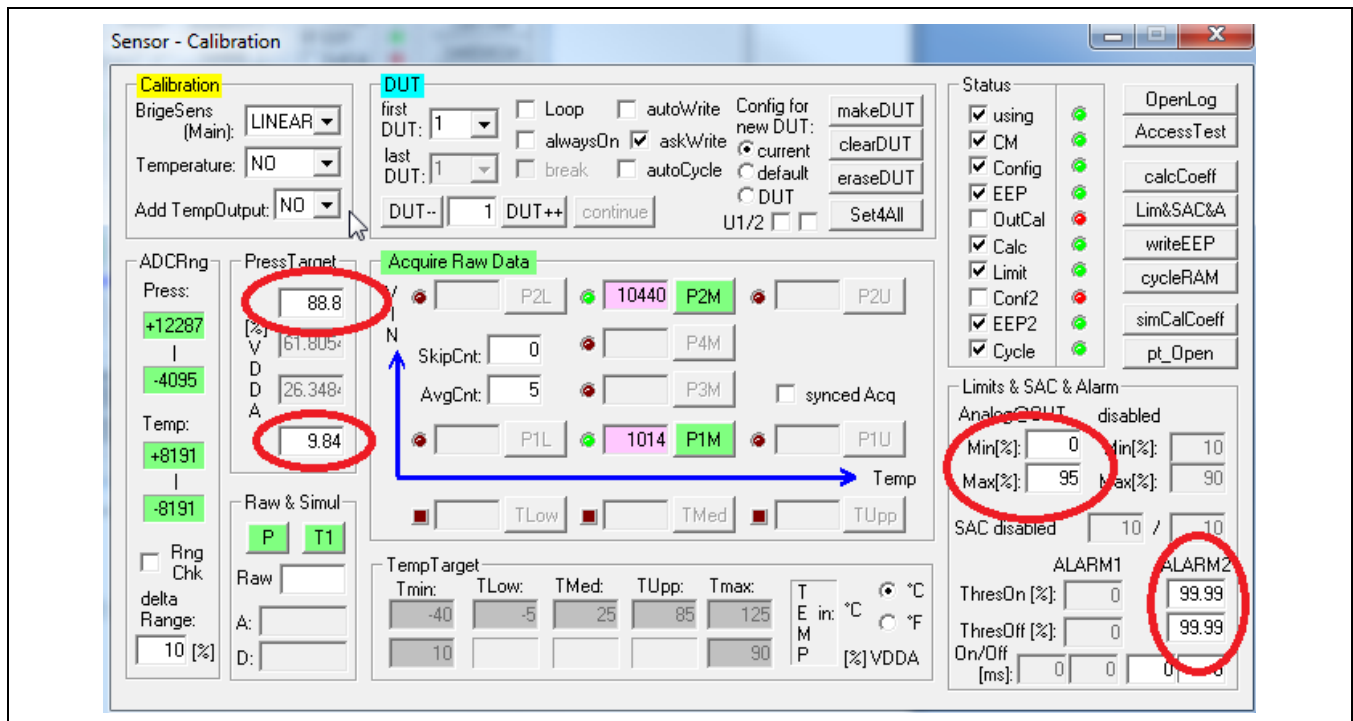
$$New_Target = Initial_Target - \left(\frac{V_{OUT} - V_{SET}}{V_{SET_MAX} - V_{SET_MIN}} \right) * (Target_max\% - Target_min\%) \quad (2)$$

For example, re-calculation of the maximum target can be done based on the measured output 10.15V and initial calibration targets 10% and 90% as demonstrated in equation (3):

$$New_Target = 90\% - \left(\frac{10.15V - 10V}{10V - 0V} \right) * (90\% - 10\%) = 88.8\% \quad (3)$$

For adjustment of the minimum signal calibration target, the sensor signal must be set to a level that results in 10% output or 1.11V for the above example (considering that 10V equals 90% output). After raw data acquisition, the above formula for calculating the adjusted targets can be applied for fine-tuning the output.

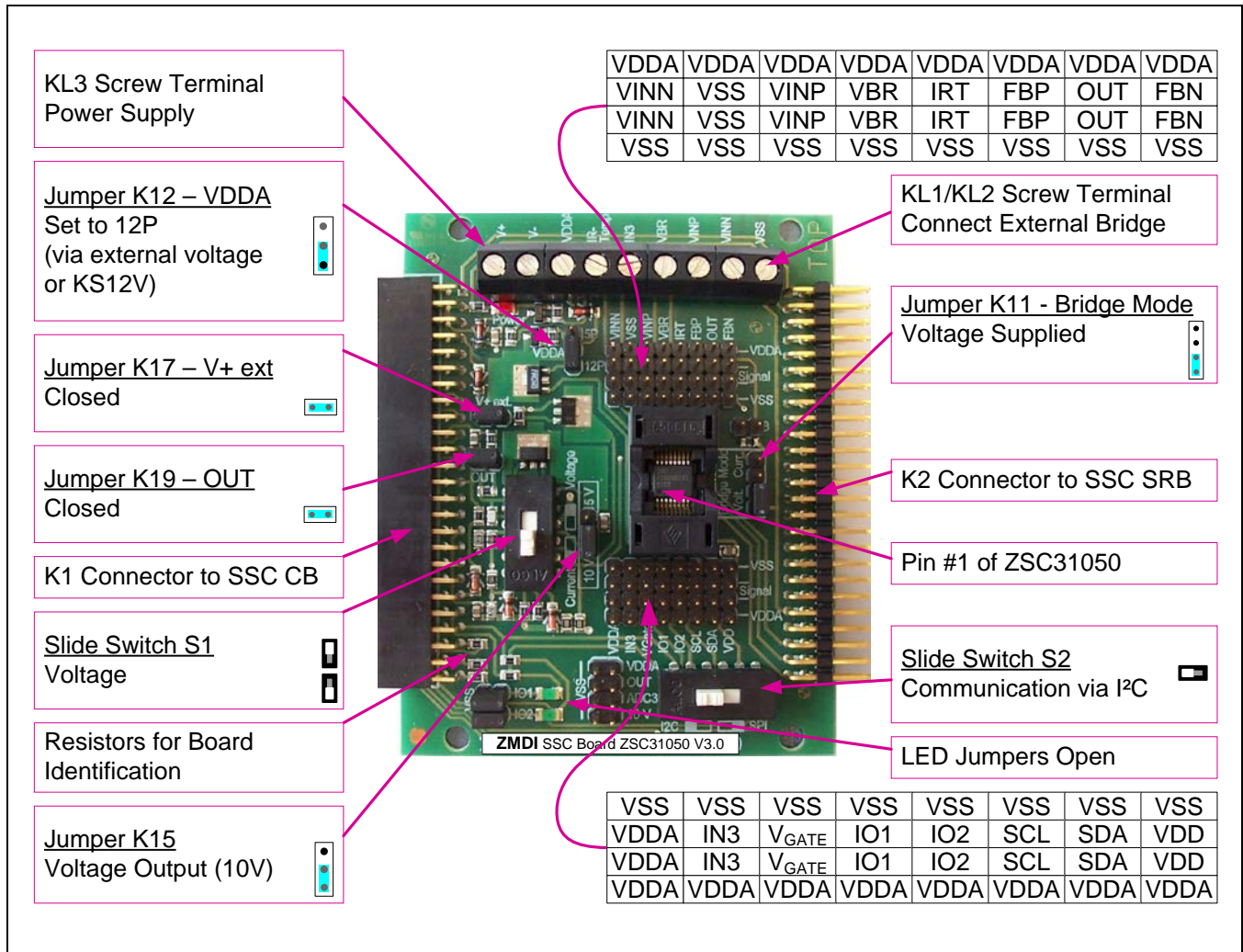
Figure 2.4 Calibration Window



2.5. Setup for the ZSC31050 Evaluation Board

Set the switches and jumpers on the SSC Evaluation Board according to Figure 2.5.

Figure 2.5 ZSC31050 Evaluation Board Settings



3 External Components

Table 3.1 Parameters for External Parts

Part ID	Ratiometric Output	Non-ratiometric Output (VOUT_NR)	Current Loop Output
R1	Not placed	3 k Ω	0 Ω
R2	Not placed	6.8 k Ω	0 Ω
R3	0 Ω	0 Ω	50 Ω
R4	Not placed	2.2 k Ω	2.2 k Ω
R5	Not placed	1 k Ω	150 Ω
R6	Not placed	390 Ω	0 Ω
R7	0 Ω	2.2 k Ω	Not placed
R8	Not placed	Typical 100 Ω (for current limitation)	Not placed
R9	Not placed	220 k Ω	220 k Ω
R10	Not placed	10 k Ω	10 k Ω
R11	Not placed	100 Ω	100 Ω
R12	Not placed	10 k Ω	10 k Ω
R13	Not placed	390 Ω	390 Ω
R14	Not placed	4.7 Ω	4.7 Ω
RC1	0 Ω	100 nF	Not placed
RC2	15 nF	2 k Ω	0 Ω
C1	100 nF		
C2	100 nF		
C3	Not placed	220 pF	220 pF
C4	Not placed	10 nF	10 nF
D1	Not placed	e.g. LL4148	e.g. LL4148
D2	Not placed	BZV55C6V8	BZV55B7V5
D3	Not placed	1N4148	Not placed
D4	LED 0603	LED 0603	LED 0603
D5	Not placed	LED 0603	LED 0603
T1	Not placed	DN3545N8 (SOT89)	DN3545N8 (SOT89)
T2	Not placed	BC817-40 (SOT23)	BC817-40 (SOT23)
T3	Not placed	BC807-40 (SOT23)	Not placed
T4	FDC6306P	FDN5618P	Not placed
T5	Not placed	BC817-40 (SOT23)	BC817-40 (SOT23)
T6	Not placed	BC817-40 (SOT23)	BC817-40 (SOT23)

4 Related Documents

Document
<i>ZSC31050 Data Sheet</i>
<i>ZSC31050 Functional Description</i>
<i>ZSC31050 Application Note – Two-Wire Current Loop Output</i>
<i>ZSC31050 Evaluation Kit Description</i>
<i>ZSC31050 Gerber Example Files</i>

Visit the ZSC31050 product page (www.IDT.com/ZSC31050) or contact your nearest sales office for the latest version of these documents.

5 Glossary

Term	Description
OWI	One-Wire Interface
SSC	Sensor Signal Conditioner

6 Document Revision History

Revision	Date	Description
1.00	September 21, 2009	First release.
1.01	April 8, 2010	Changed to IDT template.
1.10	April 5, 2011	Changed ZACwire™ description to OneWire, IDT template. Updated contact information. Renamed ZMD31050 to ZSC31050.
2.00	May 22, 2013	Schematic for three-wire operation added. Update for contact information, imagery for cover and headers.
2.10	October 14, 2013	Addition of sections 2.3, 2.4, and 2.5. Update to "Related Documents" section to add example Gerber files available on the IDT website. Update for Figure 2.3. Update for Table 3.1. Minor edits for clarity.
	April 26, 2016	Changed to IDT branding.



Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138
www.IDT.com

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com/go/sales

Tech Support
www.IDT.com/go/support

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